

WHAT IS CLAIMED IS:

1 1. An integrated circuit comprising a plurality of dynamically adjustable
2 impedance termination circuits that are coupled together in parallel to a first pin, each of the
3 impedance termination circuits comprising:

4 first resistors coupled in parallel;
5 a second resistor coupled in series with the first resistors;
6 first pass gates each coupled in series with one of the first resistors and each
7 coupled to a first control signal; and
8 a second pass gate coupled to the first pass gates and coupled to receive a
9 second control signal.

1 2. The integrated circuit according to claim 1 wherein the first resistors
2 comprise three resistors coupled in parallel.

1 3. The integrated circuit according to claim 1 wherein the integrated
2 circuit comprises three of the impedance termination circuits coupled together in parallel to
3 the first pin.

1 4. The integrated circuit according to claim 1 wherein each of the first
2 pass gates and the second pass gates comprise a p-channel transistor and an n-channel
3 transistor coupled together in parallel.

1 5. The integrated circuit according to claim 1 wherein the integrated
2 circuit includes a second set of impedance termination circuits that are coupled together in
3 parallel to a second pin, the first and the second pin being differential input/output pins.

1 6. A method for providing dynamically adjustable on-chip termination
2 impedance to a first input/output pin on an integrated circuit, the method comprising:
3 controlling first current paths through first on-chip resistors that coupled
4 together in parallel using first pass gates, each first pass gate being coupled in series with one
5 of the first on-chip resistors;
6 providing a second current path through the first on-chip resistors and a
7 second on-chip resistor that is coupled in series with the first on-chip resistors by turning ON
8 a second pass gate;

9 providing a third current path through a third on-chip resistor that is coupled in
10 parallel with the first and the second on-chip resistors by turning ON a third pass gate,
11 wherein the second and the third resistors are coupled to the first pin;
12 sensing the on-chip termination impedance; and
13 dynamically adjusting the on-chip termination impedance by changing states
14 of the first pass gates.

1 7. The method of claim 6 further comprising:
2 coupling fourth on-chip resistors together in parallel by turning ON fourth
3 pass gates, each fourth pass gate being coupled in series with one of the fourth resistors,
4 wherein the fourth on-chip resistors are coupled in series with the third resistor
5 and the second current path flows through the fourth resistors.

1 8. The method of claim 7 further comprising:
2 blocking current through a fifth resistor coupled in parallel with the first and
3 the second on-chip resistors by turn OFF a fifth pass gate.

1 9. The method of claim 7 further comprising:
2 blocking current through a selected one of the fourth resistors by turning OFF
3 one of the fourth pass gates that is coupled to the selected fourth resistor.

1 10. The method of claim 6 further comprising:
2 blocking current through a selected one of the first resistors by turning OFF
3 one of the first pass gates that is coupled the selected first resistor.

1 11. The method of claim 6 further comprising:
2 decoupling a third on-chip resistor from the first on-chip resistors by turning
3 OFF a third pass gate; and
4 blocking a fourth current path through a fourth on-chip resistor that is coupled
5 in parallel with the first and the second on-chip resistors by turning OFF a fourth pass gate.

1 12. The method of claim 6 wherein the integrated circuit is a field
2 programmable gate array.

1 13. The method of claim 6 further comprising providing on-chip
2 termination impedance to a second input/output pin on the integrated circuit by:

3 coupling fourth on-chip resistors together in parallel by turning ON fourth
4 pass gates, each fourth pass gate being coupled in series with one of the fourth on-chip
5 resistors;
6 providing a fourth current path through the fourth on-chip resistors and a fifth
7 on-chip resistor coupled in series with the fourth on-chip resistors by turning ON a fifth pass
8 gate,
9 wherein the first and the second pins are differential pins.

1 14. An integrated circuit comprising a first dynamically adjustable on-chip
2 impedance termination circuit, wherein the first impedance termination circuit comprises:
3 means for coupling together first resistors in parallel in response to first
4 control signals;
5 means for providing a first current path through a second resistor coupled in
6 series with the first resistors in response to a second control signal; and
7 means for providing a second current path through a third resistor coupled in
8 parallel with the first resistors and the second resistor in response to a third control signal,
9 wherein the first, second, and third resistors provide termination impedance at a pin.

1 15. The integrated circuit as defined in claim 14 further comprising:
2 means for blocking current through a fourth on-chip resistor that is coupled to
3 the second and the third on-chip resistors in response to a fourth control signal.

1 16. The integrated circuit as defined in claim 14 further comprising:
2 means for blocking current flow through one of the first resistors in response
3 to a changed value of a corresponding one of the first control signals.

1 17. The integrated circuit as defined in claim 14 wherein the integrated
2 circuit further comprises a second on-chip impedance termination circuit coupled to the first
3 on-chip impedance termination circuit, wherein the second impedance termination circuit
4 comprises:
5 means for coupling together fourth resistors in parallel in response to fourth
6 control signals;
7 means for providing a third current path through a fifth resistor coupled in
8 series with the fourth resistors in response to a fifth control signal; and

9 means for providing a fourth current path through a sixth resistor coupled
10 parallel with the fourth resistors and the fifth resistor in response to a sixth control signal,
11 wherein the fourth, fifth, and sixth resistors provide termination impedance at a second pin.

1 18. The integrated circuit as defined in claim 14 wherein the integrated
2 circuit is a programmable logic device.

1 19. The integrated circuit as defined in claim 14 further comprising:
2 means for coupling together fourth resistors in parallel in response to fourth
3 control signals, wherein the second current path flows through the third and the fourth
4 resistors.

1 20. The integrated circuit as defined in claim 19 further comprising:
2 means for providing a third current path through a fifth resistor coupled
3 parallel with the fourth and the third resistors in response to a fifth control signal.